Disclosure FIS8-[redacted]-0323

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Created By DURESETI CHIDAMBARRAO On [redacted] 11:10:00 AM EDT
Last Modified By DURESETI CHIDAMBARRAO On [redacted] 08:41:32 AM EDT

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***Title of disclosure (in English)**
Strained Si on SI:C-OI and SGOI

Summary

Status		Under Evaluation
Final Deadline		
Final Deadline Reason		
*Processing Location		Fishkill
*Functional Area	select	(DKL) DKL ... ABERNATHEY: 256MB DRAM "Non-Alliance" Only
Attorney/Patent Professional		Joseph P Abate/Fishkill/IBM
IDT Team	select	Oleg Gluschenkov/Fishkill/IBM William Devine/Fishkill/IBM DOMINIC SCHEPIS/Fishkill/IBM David Hanson/Fishkill/IBM Thomas Dyer/Fishkill/IBM Noah Zamdmer/Fishkill/IBM DURESETI CHIDAMBARRAO/Fishkill/IBM Werner Rausch/Fishkill/IBM Samuel Fung/Fishkill/IBM
Submitted Date		[redacted]
*Owning Division	select	TG
Incentive Program		
Lab		
*Technology Code		101N2
PVT Score		

Inventors with a Blue Pages entry

Inventors: DURESETI CHIDAMBARRAO/Fishkill/IBM, Omer Dokumaci/Fishkill/IBM, Oleg Gluschenkov/Fishkill/IBM

Inventor Name	Inventor Serial	Div/Dept	Inventor Phone	Manager Name
> Chidambarrao, Dureseti (Chidu)	254149	29/38WA	532-2336	Divakaruni, Rama
Dokumaci, Omer H.	795369	29/62GD	532-4893	Oldiges, Philip (Phil)
Gluschenkov, Oleg G.	2A1177	29/BIXA	532-9788	Sekiguchi, Akihisa (Aki)

> denotes primary contact

Inventors without a Blue Pages entry

IDT Selection

Attorney/Patent Professional	Joseph P Abate/Fishkill/IBM
IDT Team	Oleg Gluschenkov/Fishkill/IBM William Devine/Fishkill/IBM DOMINIC SCHEPIS/Fishkill/IBM David Hanson/Fishkill/IBM Thomas Dyer/Fishkill/IBM Noah Zamdmer/Fishkill/IBM DURESETI CHIDAMBARRAO/Fishkill/IBM Werner Rausch/Fishkill/IBM Samuel Fung/Fishkill/IBM
Response Due to IP&L	[redacted]

***Main Idea**

1. Background: What is the problem solved by your invention? Describe known solutions to this problem (if any). What are the drawbacks of such known solutions, or why is an additional solution required? Cite any relevant technical documents or references.

Stresses are known to affect device drive currents. There have been many proposals to improve both nFET and pFET device performance using tensile and compressive stresses, respectively, which include modulating spacer intrinsic stresses and STI material changes individually for the two MOSFETs using masks.

Tensilely strained Si on relaxed SiGe has also been proposed as a means to apply this stress. Unfortunately it can apply only biaxial tensile stress on the Si cap as used in stack form. This constrains the regime of Ge% that is useful because of the nature of pFET sensitivity to stress. The nFET performance monotonically improves with biaxial tension. However, the pFET is degraded with biaxial tension until about 3GPa at which point it begins to improve. In order to improve both the pFET and nFET simultaneously the Ge% needs to be high > 25-30% (or equivalently > 3-4GPa in stress). This level of Ge% is hard to implement into processes and is not very manufacturable with major Issues including (just to name a few) surface roughness, process complexity, defect and yield control. Therefore, it would be useful to have the lower Ge% regime for the nFET (say 10-20% which still provides a significant boost) while at same time getting significant compression for the pFET. Given that we cannot use this Ge% for the pFET (since it would be detrimental for the pFET because of the relatively lower levels of tension, <3GPa range), we need something else in the pFET.

The stress state where pFET shows continued improvement is on the compressive side. In this invention we show a different approach to apply tension and compression to nFETs and pFETs, respectively, a major facilitating factor being Si:C for which we give a background summary below.

Background Information on Si:C

Si:C is known to grow epitaxially on Si where it is inherently tensile. A 1% C content in a Si:C/Si material stack can cause tensile stress levels in the Si:C on the order of 500MPa. In comparison, in the SiGe/Si system about 6% Ge is needed to causes a 500MPa compression. This 1% level of C can be readily incorporated into Si during epitaxial growth as shown in Ernst et al, VLSI Symp., 2002, p92.

In Ernst et al, they make use of Si/Si:C/Si layered channels for nFETs. However, their Si:C part of the structure is not relaxed. Instead they are using the unrelaxed Si:C as part of the channel itself with a vey thin Si cap. The problem with this approach is that the mobility was not enhanced, but retarded, depending on the C content, from scattering. In this invention we use SIGe srelaxed layers for the nFET and Si:C

layers for the pFET.

Invention

In SGOI, one approach is to obtain the SiGe through thermally mixing a deposited Ge layer into the SOI thin film. The process envisioned for this invention retains this ability for the nFET but modifies it for the pFET. Instead of SiGe we get Si:C for the pFET. Clearly both the method and structure are invented here.

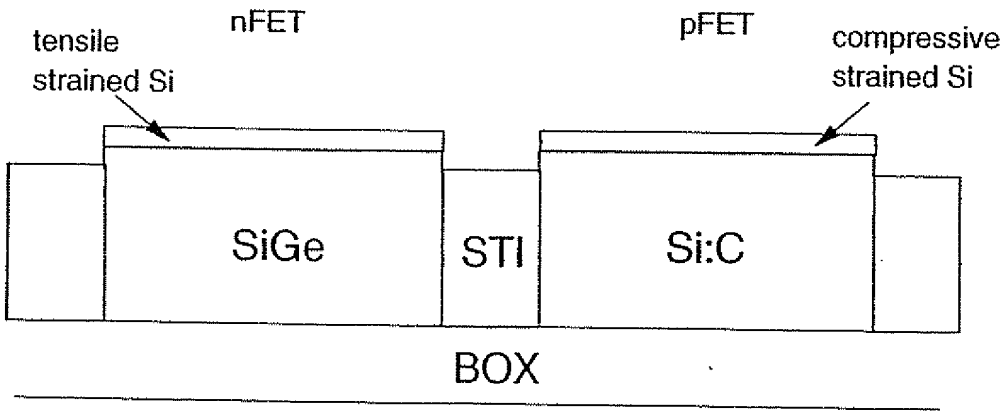
Furthermore, placement of at least two crystal islands with different relaxed crystal lattice (different dimensions between the atoms) was only feasible by wafer bonding techniques where the islands have a relatively large size. The proposed methods yields a unique substrate with small crystal islands which have a fully relaxed but different crystal structure. The nontrivial enabling element of such novel structure is the use of high-temperature stable amorphous material (e.g. SiO2) in between the islands and the crystal-on-insulator structure.

The unique substrate with different crystal islands allows for the placement of differently strained layers of optionally different crystals. In the first set of embodiments which are described below, the differently strained layers are tensile and compressive Si layers. In a 2nd set of embodiments (which are a simple extension of the descriptions below by omitting the strained silicon deposition on one of the islands), the different layers are a tensile Si layer and SiGe layer or compressive Si layer and Si:C layer.

2. Summary of Invention: Briefly describe the core idea of your invention (saving the details for questions #3 below). Describe the advantage(s) of using your invention instead of the known solutions described above.

The main conceptual point of this invention is to get the SiGe and Si:C structures for the nFET and pFET, respectively. We show how to integrate Si:C and SiGe into the thermally mixed method. The structure is seen in Figure 1 below.

Figure 1: Final Strained Si structure



Generalized Claim

This invention has a seminal and important contribution to the art of making substrates with semiconductor islands on insulator with multiple crystal lattice constants. The general claim includes forming "relaxed" islands of semiconductor that have different lattice constants: island 1 being crystal 1 having lattice constant a >= aSi and island 2 being crystal 2 having lattice constant a <= aSi.

The example shown above in Figure 1 is one where we use SiGe and Si:C for crystal 1 and 2, respectively. One can grow selective Si epi on this substrate which will strain tensilely and compressively on SiGe and Si:C respectively. Let us call these materials crystal 3 and crystal 4 respectively. This particular application is suitable for strained planar nFETs or pFETs.

Holes are known to have excellent mobility in SiGe, but reliable thermal-based oxides are hard to form on this material. However, if the dielectric (some high K material for example) can be deposited then we would be using just relaxed SiGe crystal 1 for pFETs in tandem with crystal 1 (again relaxed SiGe) with tensilely strained crystal 3 epi for the nFET. This invention generalizes to the concept of multiple lattice constant islanded substrates.

One important enabling feature is the STI before high temparature thermal mixing anneal which provides more or less complete stress relief for the substrate and therefore enables the lattice changes in the islands to fully relaxed SiGe or Si:C.

Advantages

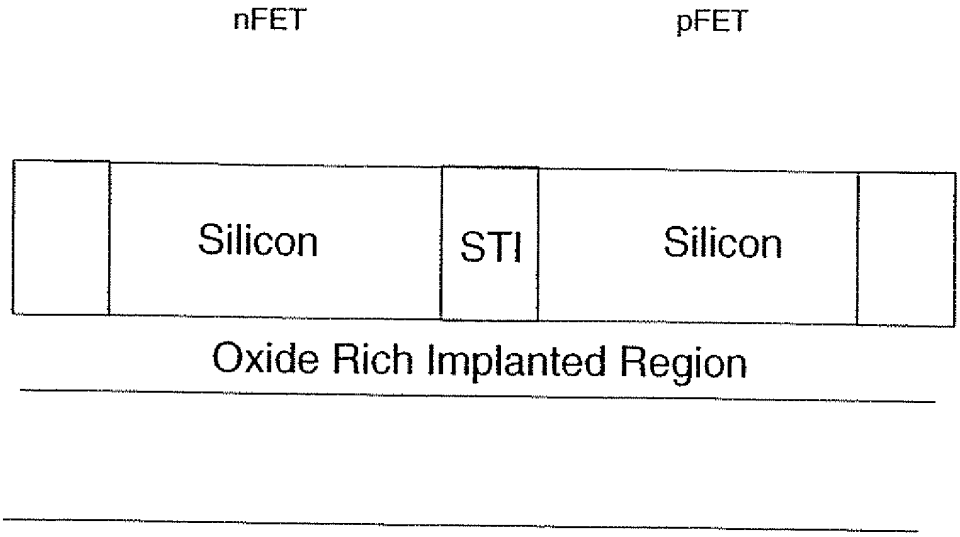
(i) The Ge% needed is not as large to cause defect issues:
(ii) The relaxation of the SiGe and Si:C is even better than blanket (SiGe or Si:C) substrates since during the high temperature thermal mixing step (typically ~1300C) , the STI can relax fully and facilitate the relaxation of the SiGe and Si:C "islands" even further. This is one key differentiating feature of this approach.

3. Description: Describe how your invention works, and how it could be implemented, using text, diagrams and flow charts as appropriate.

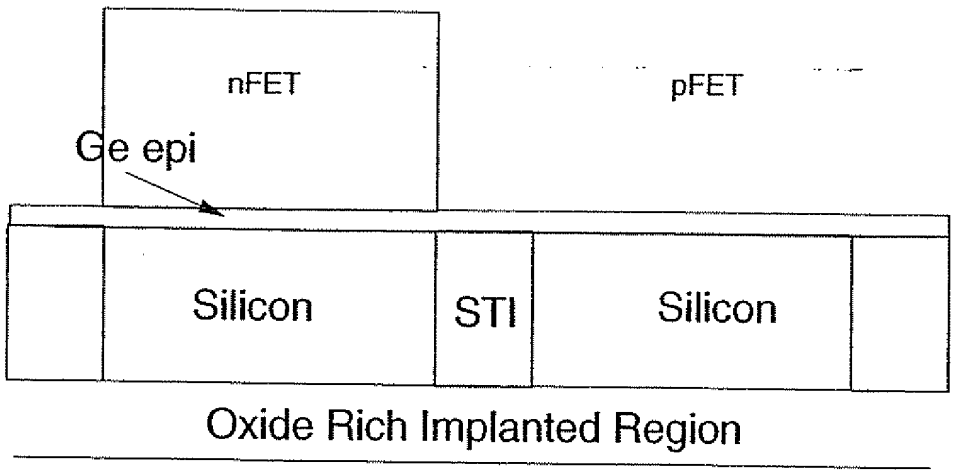
Embodiment 1

The embodiment and its associated process are seen below.

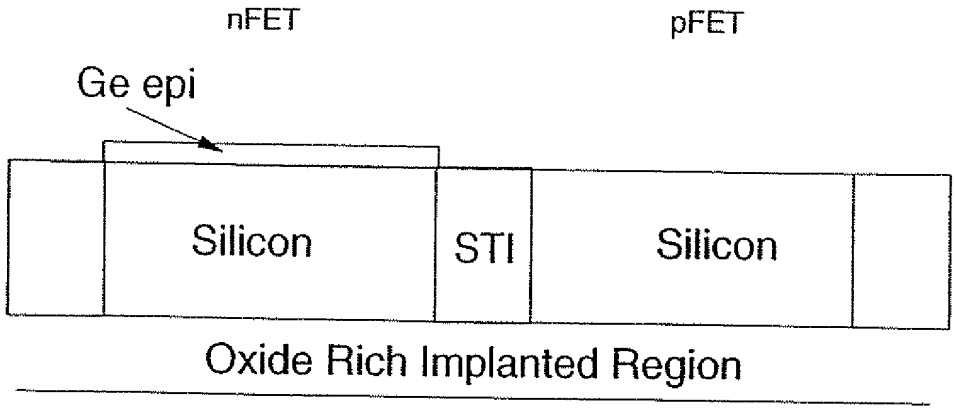
Step 1: STI formation, SIMOX Implant



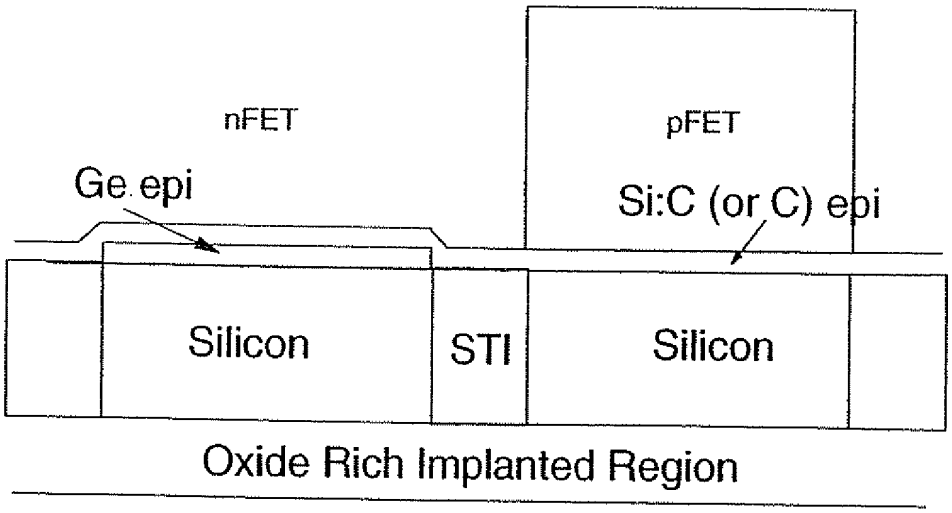
Step 2: Deposit Ge, Mask nFET RX



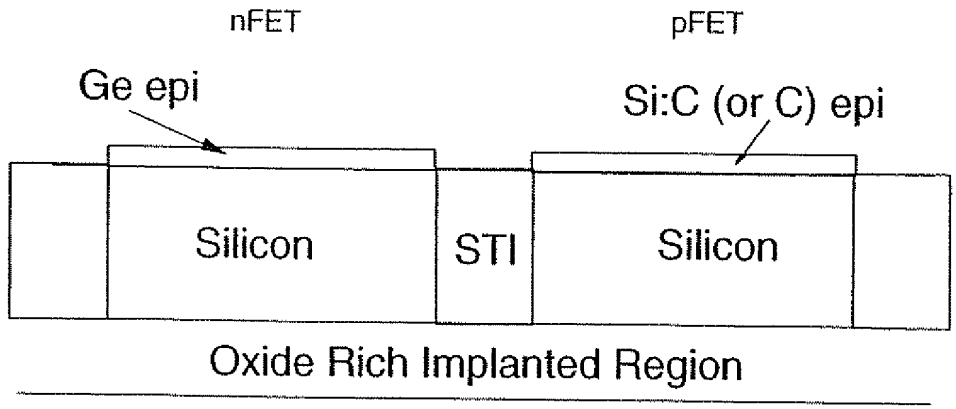
Step 3: Etch Ge from pFET regions and strip nFET RX mask



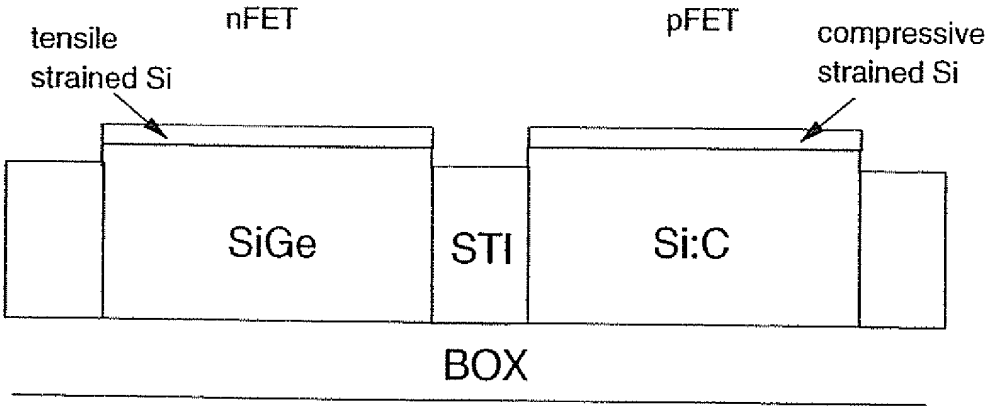
Step 4: Deposit Si:C (or C) and mask pFET RX



Step 5: Etch Si:C (or C) and strip pFET RX mask



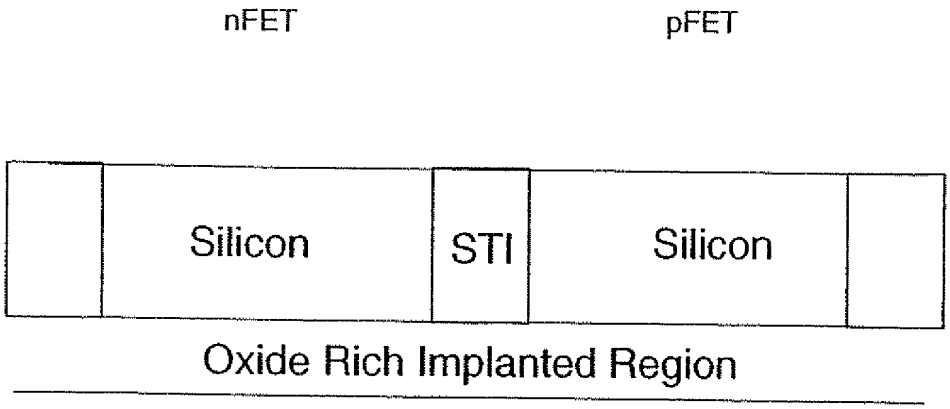
Step 6: Thermal anneal for mixing followed by selective Si epi which is strained.



Embodiment 2

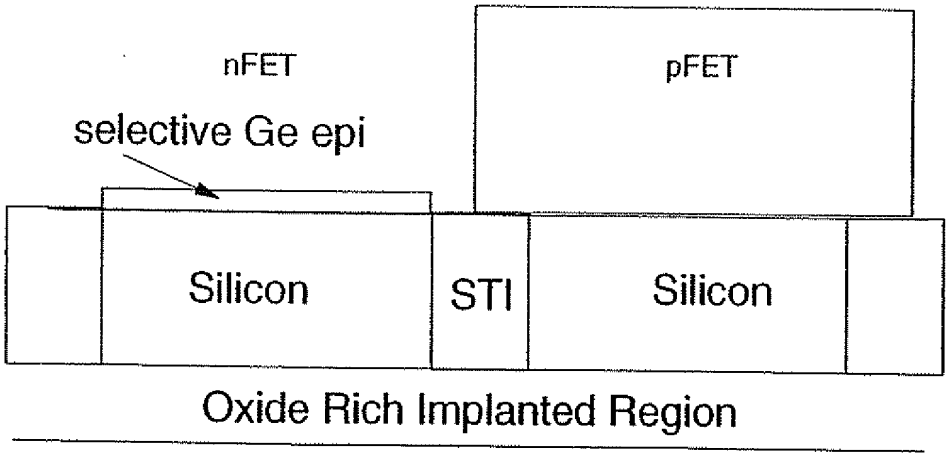
The embodiment and its associated process are seen below. Here we do selective epi rather than deposition and etch.

Step 1: STI formation, SIMOX Implant

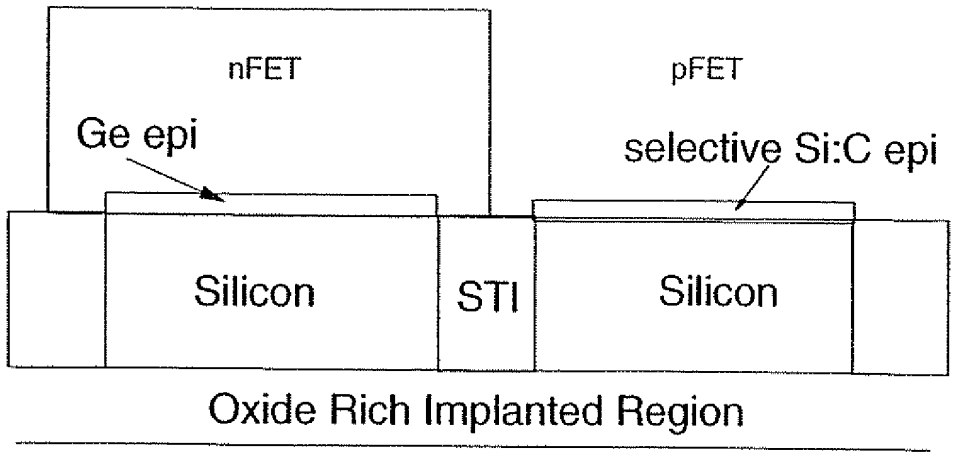


SIMOX Implant is optional. The substrate can be an SOI substrate created by any other known means such as wafer bonding techniques.

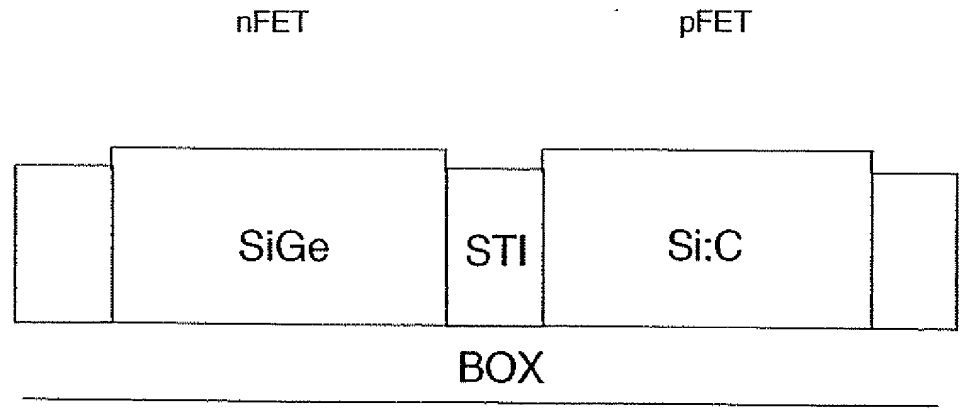
Step 2: Deposit liner, Mask pFET, etch liner, and grow selective Ge epi



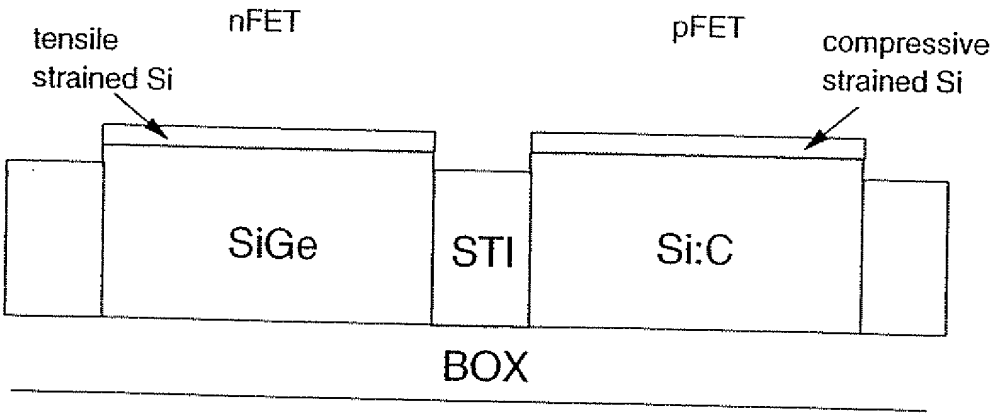
Step 3: Remove mask and pFET liner, deposit thin liner, mask nFET and grow selective Si:C epi



Step 4: Remove mask and pFET liner, thermal mixing treatment (1350C for example) forms SiGe, Si:C and BOX



Step 5: Grow selective Si which is strained



Embodiment 3

Instead of Si:C (or C) epi as seen in step 3 of the above embodiments, we can implant C at a high dose into the pFET region which can produce concentrations much greater than the 1-2% Si:C upon thermal annealing.